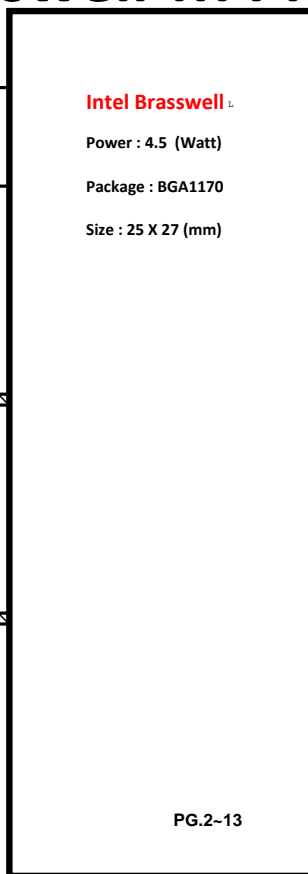


UMA (11.6")

## Intel Brasswell-M Platform Block Diagram

+3VS5/+5VS5	PG.29
MOIC	PG.31
CPU Core	PG.32,33
DDR3L	PG.30
Charger	PG.28

DDR3L	1600MT/s Channel A
Memory down*4pcs	PG.14
DDR3L	1600MT/s Channel B
Memory down*4pcs	PG.15



eDP (2 lane)

EDP panel

PG.18

DP Port0

HDMI

PG.18

USB 3.0

USB 2.0

USB 2.0

USB 2.0

USB3.0 Ports

X1

PG.23

USB2.0 Ports

X1

PG.23

eMMC 4.51

eMMC  
32G/64G

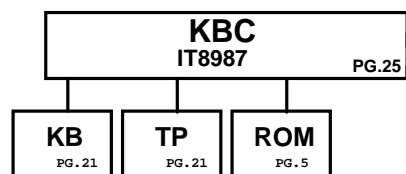
PCI-E x2

Card Reader  
RTS5239-GR

PG.17

WLAN  
BT COMBO  
NGFF M2

PG.24

WLAN  
BT COMBO  
NGFF M2

PG.24

Webcam

PG.18

WWAN  
NGFF M2

PG.20

Azalia

AUDIO  
CODEC  
ALC 3227

PG.19

Speaker

PG.19

Without amp for eMMC sku

Headphone  
amplifier  
HPA022642RTJR  
Daughter board

Combo Jack

Daughter board



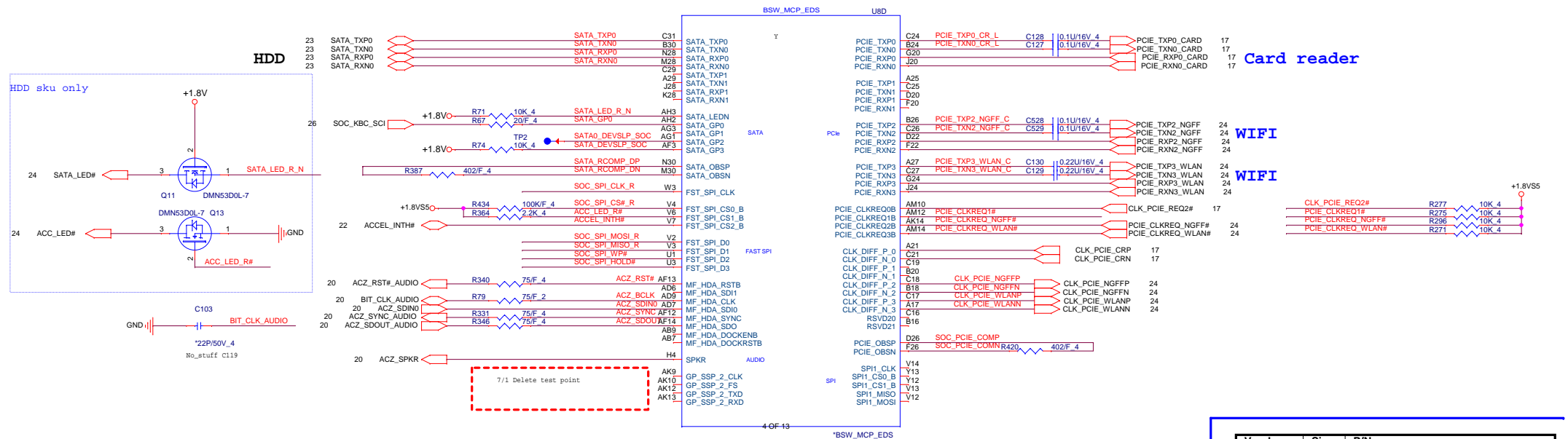
PROJECT : Y0H  
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Monday, July 06, 2015	Sheet	1 of 38

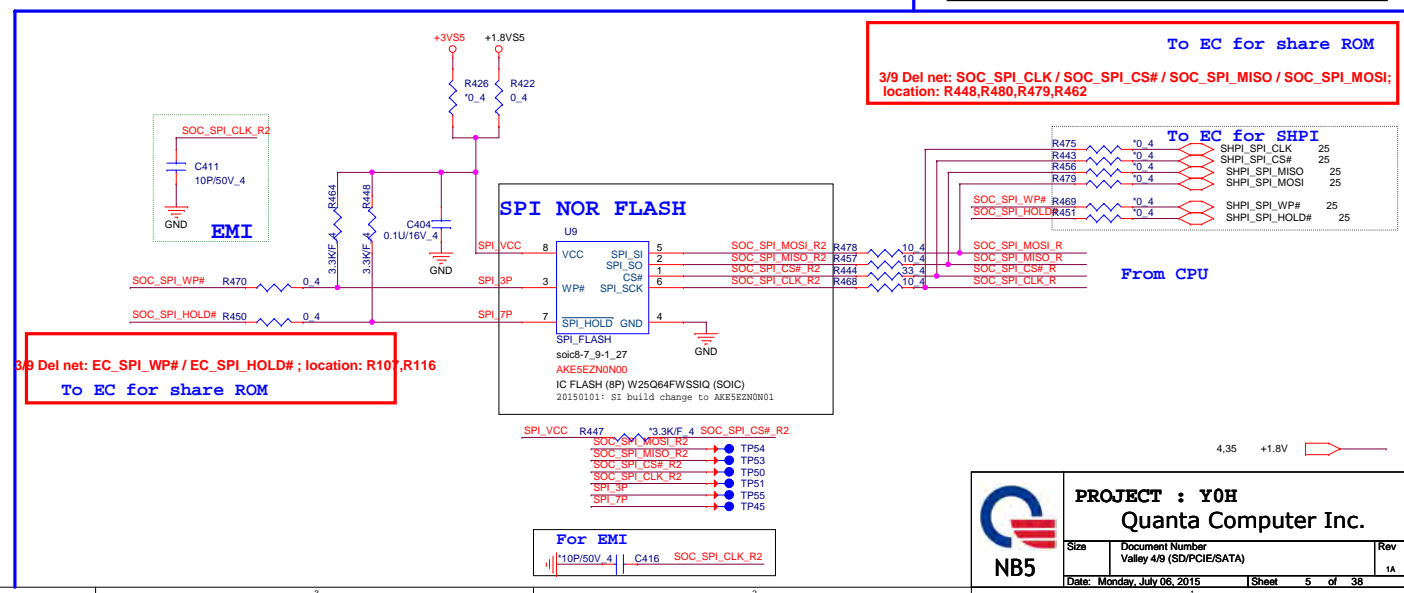






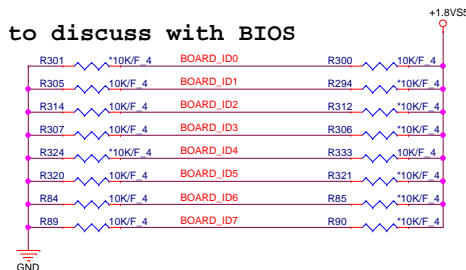


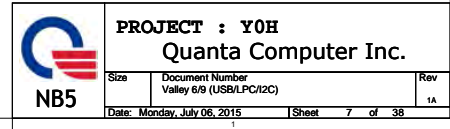
Vender	Size	P/N
Winbond	8MB	AKE5EZ2N0N01 (W25Q64FWSSIQ)
GigaDevice	8MB	AKE5EG-0Q00 (GD25LQ64CSIGR)
	8MB	AKE5EFN0Q00 (EN25S64-104HIP)
Socket (208mil)		DFHS08FS023 (Firstly Stuff)



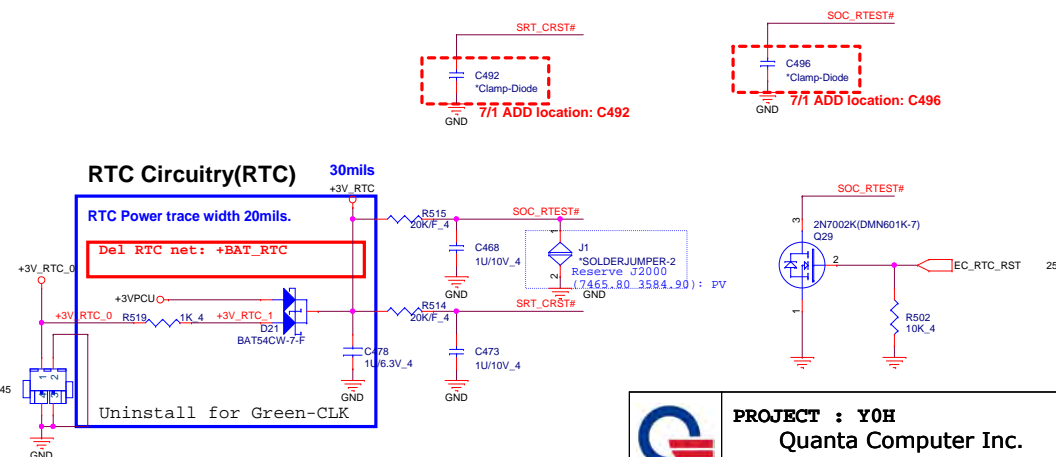
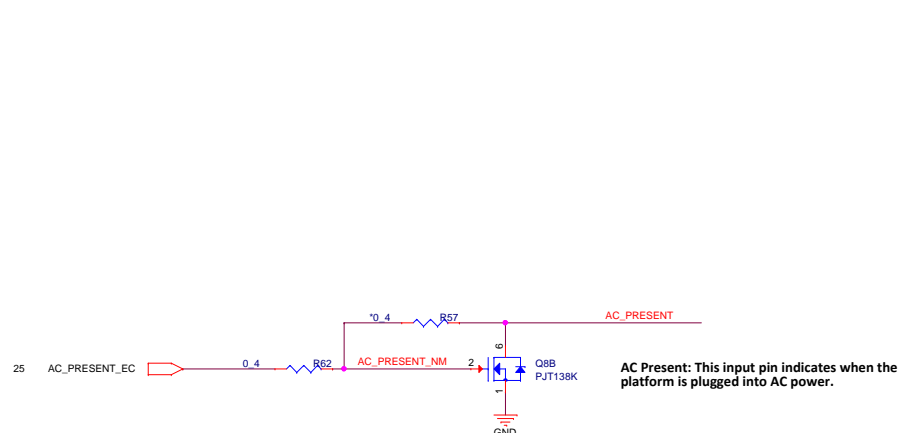
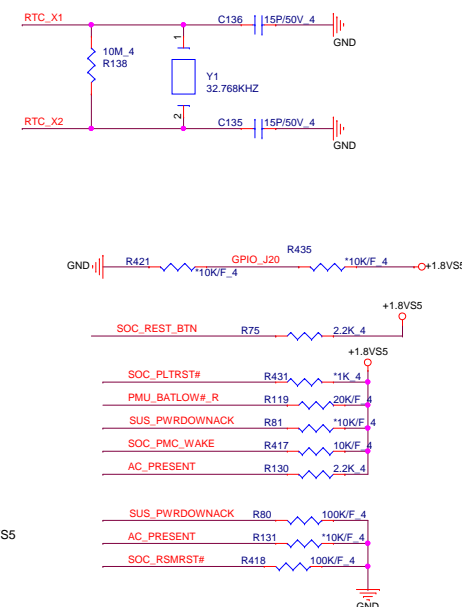
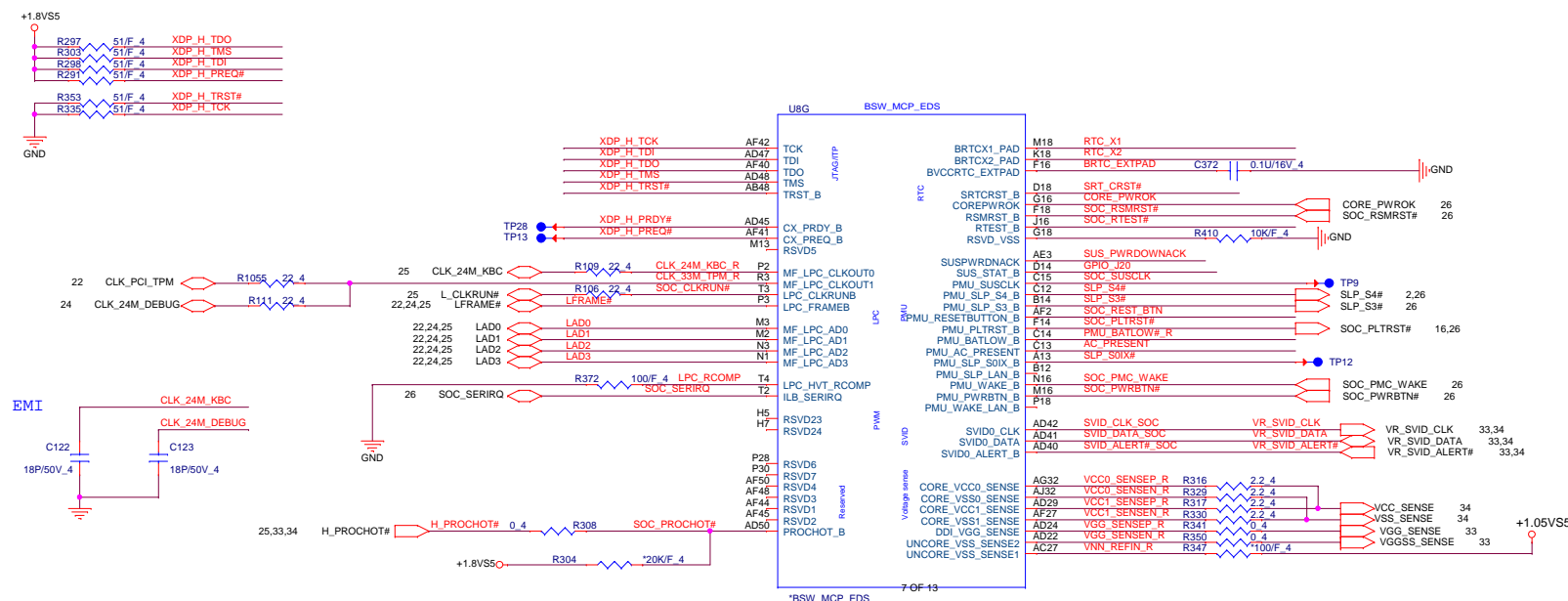


Model	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Samsung	0	1	0	2G=0	0	0	0	0 : emmc
Mircon	0	0	1	4G=1	0	0	0	1 : HDD
Hynix	0	0	0	0	0	0	0	



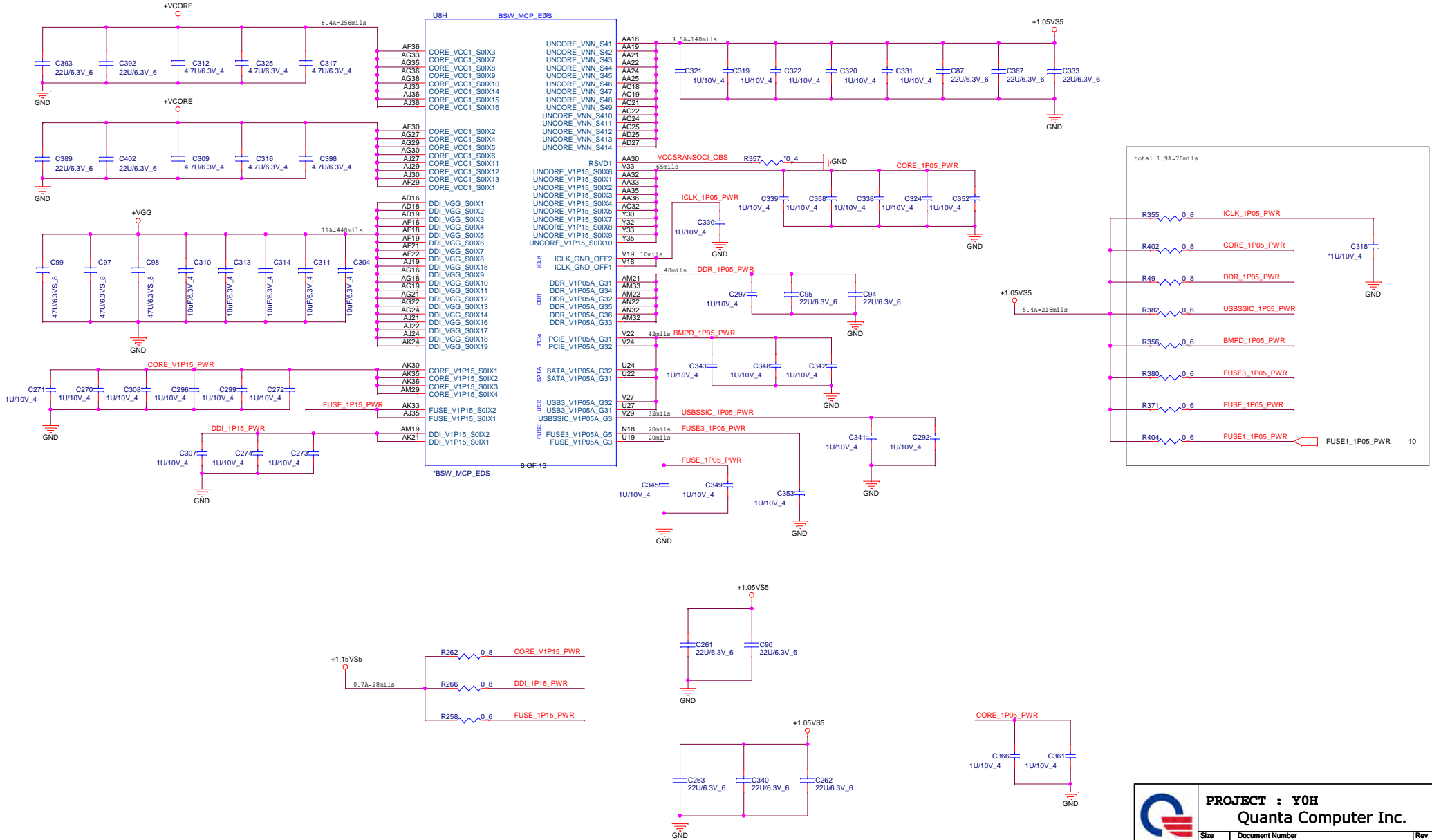


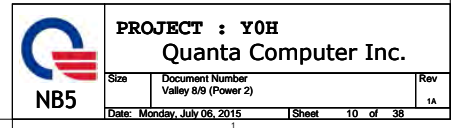
### RTC Clock 32.768KHz

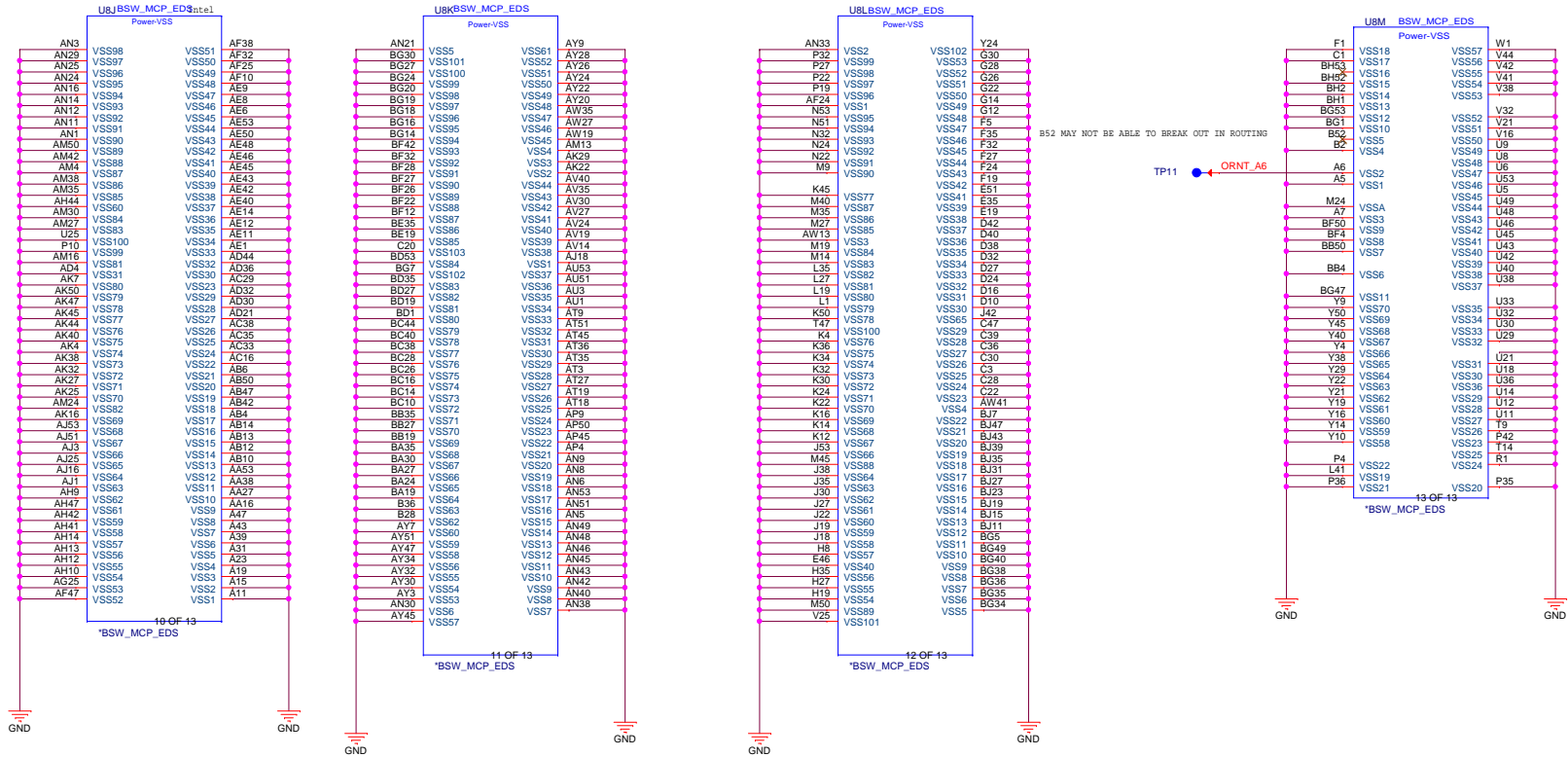


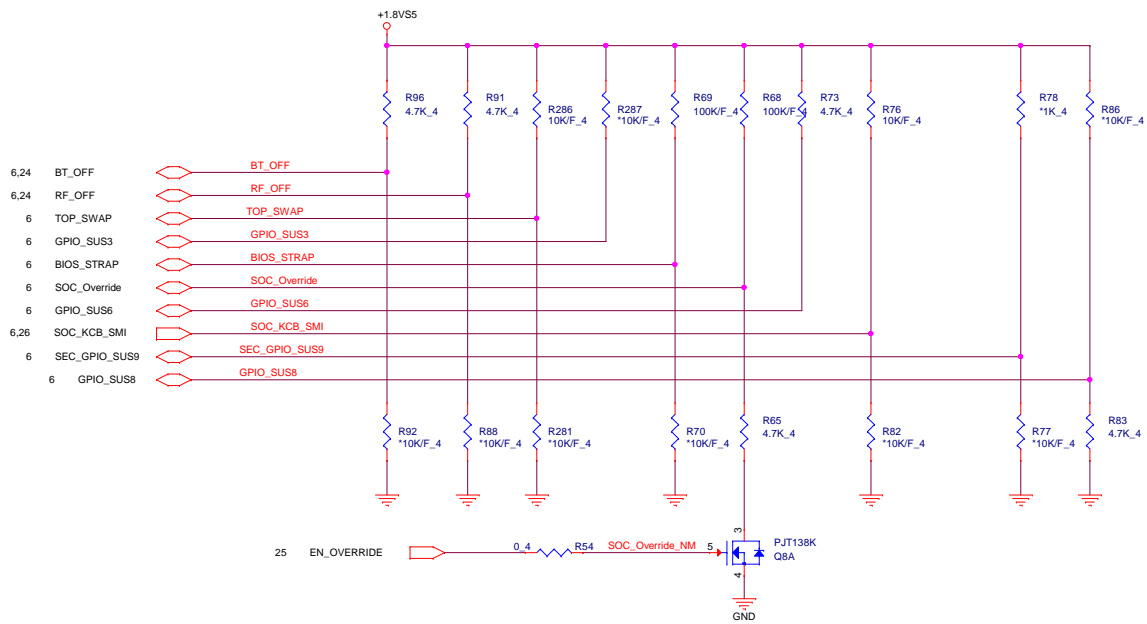


VNN can optionally be merged with V1P05A  
if display resolution is 2560 x1600 @ 60Hz or lower.

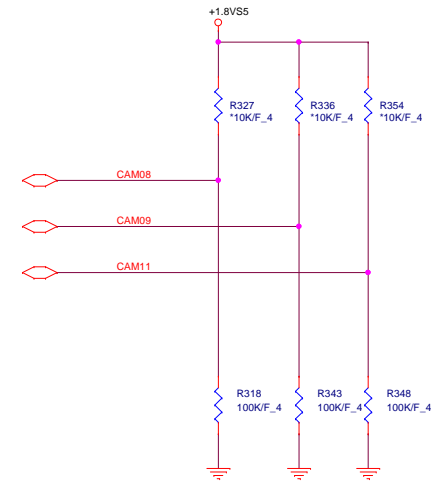








4 CAM08  
4 CAM09  
4 CAM11

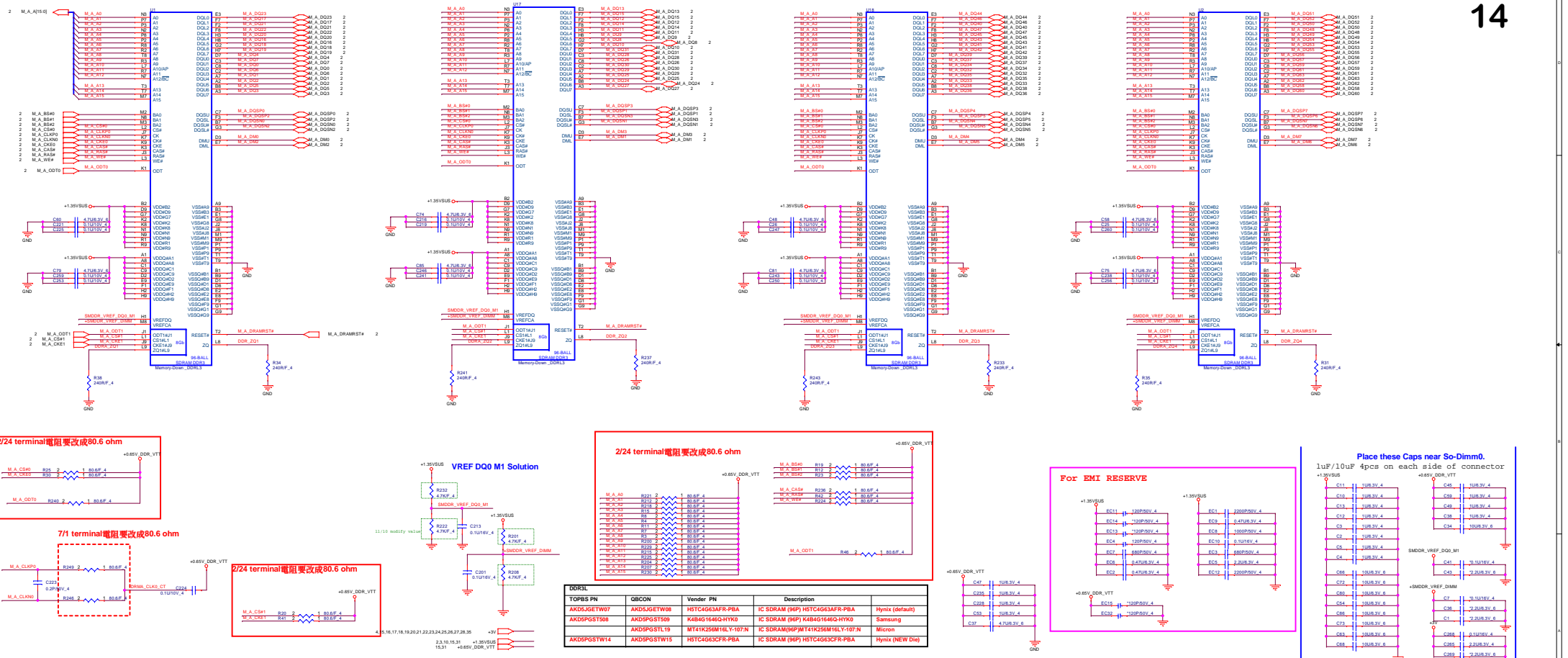


REQUIRED STRAPS

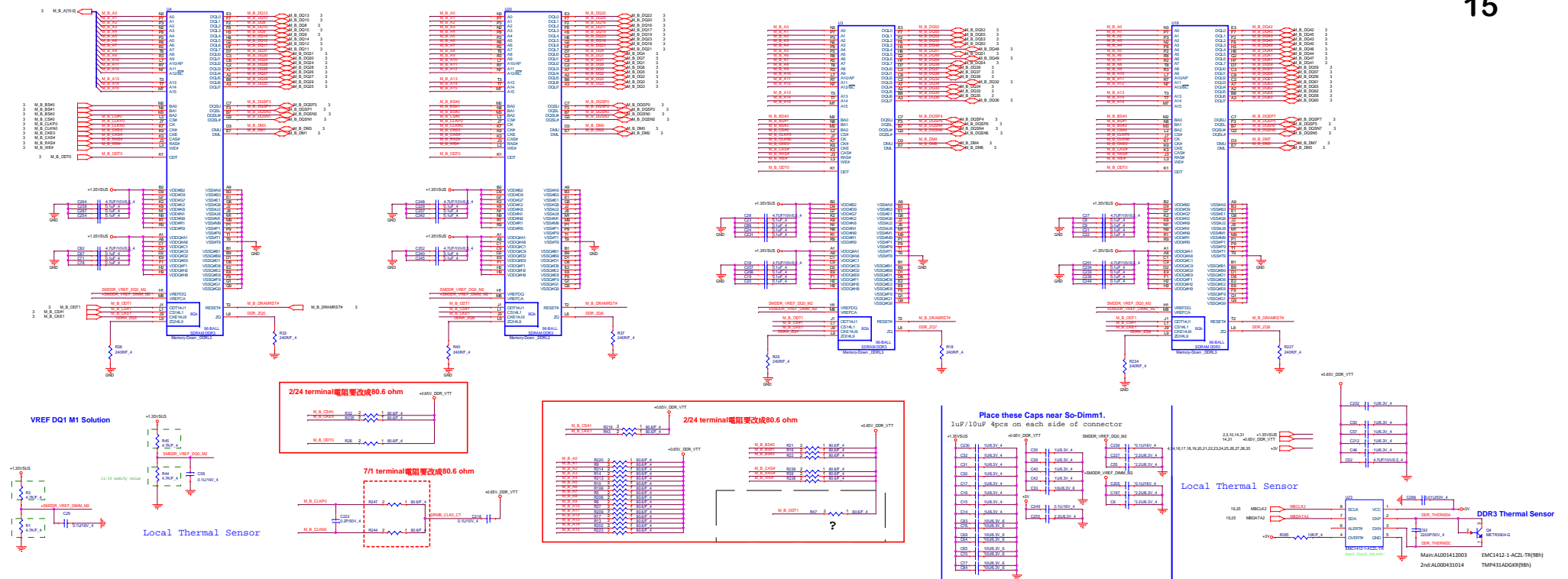
	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override DEFAULT			Supply is 1.25V DEFAULT

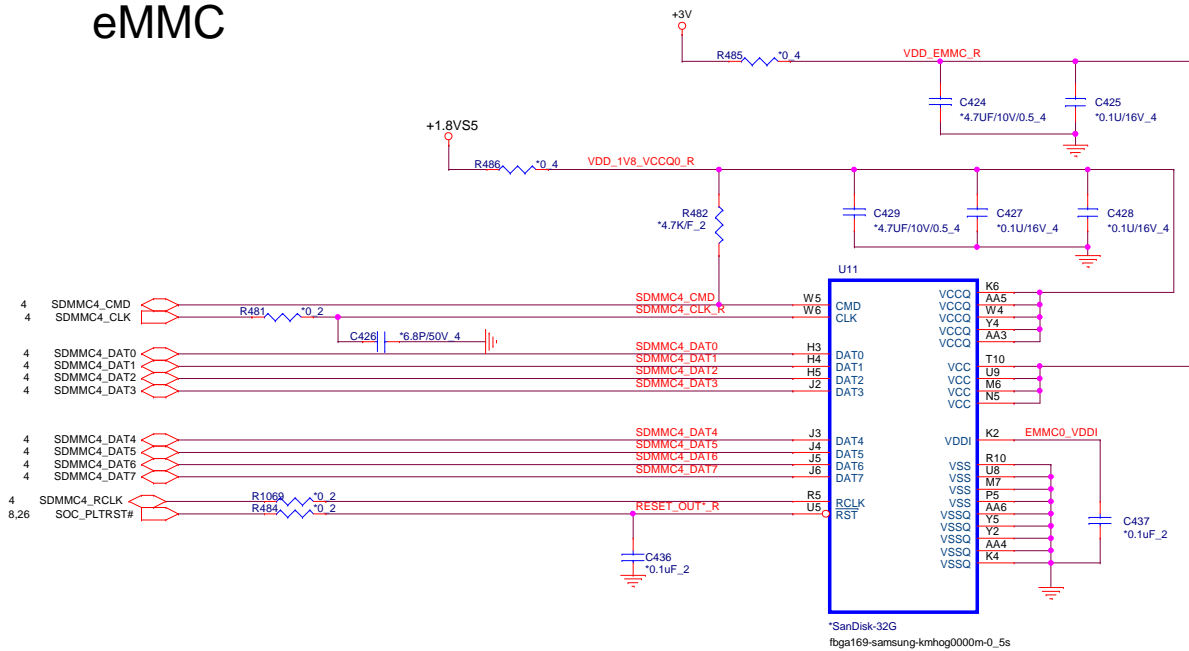
	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT





TOPSS PN	QBCON	Vender PN	Description	Hymix (default)
AKDSJGETW07	AKDSJGETW08	HSTC4G63AFR-PBA	IC SDRAM (8P) HSTC4G63AFR-PBA	Hymix (default)
AKDSPGSTW08	AKDSPGSTW09	K4B4G1646Q-HYK0	IC SDRAM (8P) K4B4G1646Q-HYK0	Samsung
AKDSPGSTW10	AKDSPGSTW11	MT41K256M16L1-Y107-N	IC SDRAM (8P) MT41K256M16L1-Y107-N	Micron
AKDSPGSTW14	AKDSPGSTW15	HSTC4G63CFR-PBA	IC SDRAM (8P) HSTC4G63CFR-PBA	Hymix (NEW line)





\*SanDisk-32G  
fbga169-samsung-kmhog0000m-0\_5s

footprint : BGA 169 - BGA 153 co-lay  
BGA 169 PIN : 14mmX18mm  
BGA 169 PIN : 12mmX16mm  
BGA 153 PIN : 11.5mmX13mm

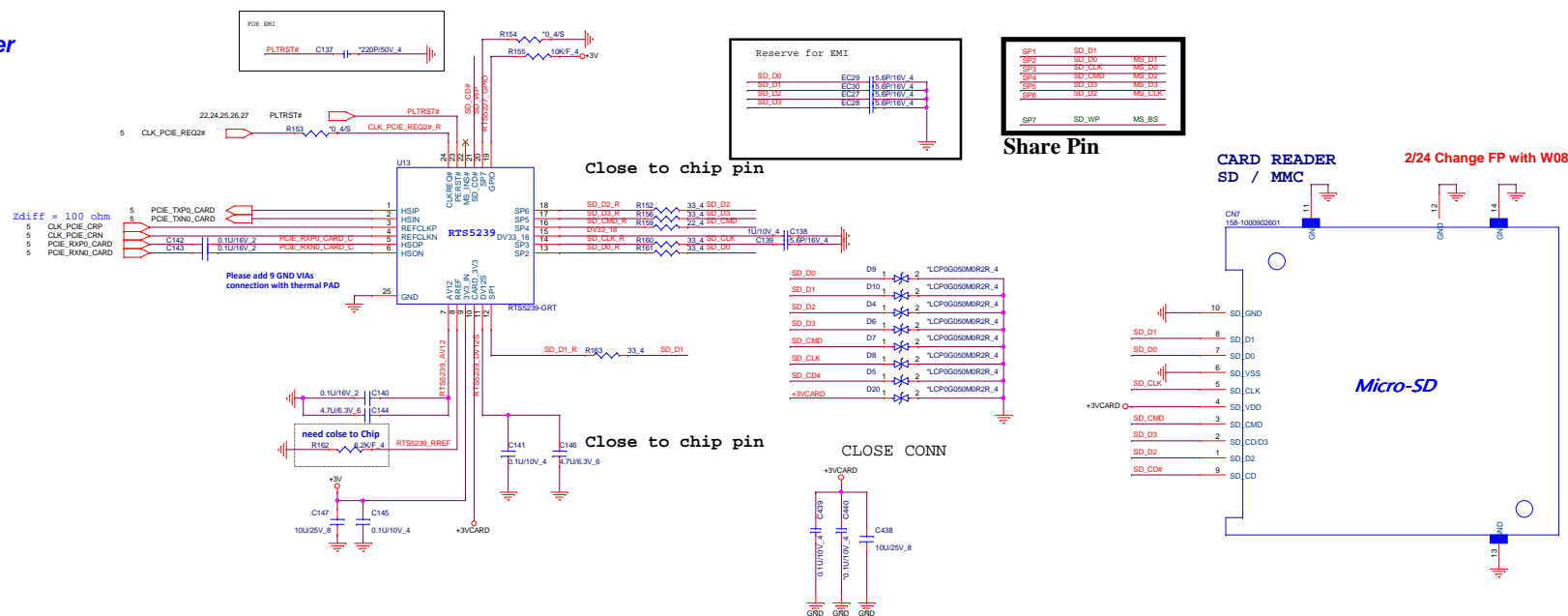
Default

iNAND (eMMC) V4.51				
TOPBSQ	QBCON	Description	SIZE	Vender
AKE3SZ-TW01	AKE3SZ-TW02	IC FLASH(153P)H26M64103EMR(FBGA)	32G	Hynix
	AKE5SZ0T512	IC FLASH(153)KLMBG4GEND-B031(FBGA)	32G	samaung
AKE3SFUT000	AKE3SFUT001	IC FLASH(153P)SDIN9DW4-32G(FBGA)	32G	SanDisk
AKE3TG-TW01	AKE3TG-TW02	IC FLASH(153P)H26M78103CCR(FBGA)	64G	Hynix
	AKE3TZPT520	IC FLASH(153)KLMCG8GEND-B031(FBGA)	64G	samaung
AKE3TFUT101	AKE3TFUT102	IC FLASH(153P)SDIN9DW4-64G(FBGA)	64G	SanDisk

eMMC setting		Location					
Vender	SIZE	R526 ~*10K_4	R528 ~*10K_4	R527 ~*10K_4	R529 ~*10K_4	R530 ~*10K_4	
Hynix	32G	1	0	0	0	0	
samaung	32G	1	1	0	0	0	
SanDisk	32G	1	1	1	0	0	
Hynix	64G	1	1	1	1	0	
samaung	64G	0	1	1	1	1	
SanDisk	64G	0	0	1	1	1	
Hynix	128G	0	0	0	1	1	
samaung	128G	0	0	0	0	1	
SanDisk	128G	0	0	0	0	0	
		1	1	1	1	1	

Memory setting		Location					
Vender	SIZE	R521 ~*10K_4	R522 ~*10K_4	R523 ~*10K_4	R524 ~*10K_4	R525 ~*10K_4	
Hynix	2G	1	0	0	0	0	
samaung	2G	1	1	0	0	0	
Micron	2G	1	1	1	0	0	
Hynix	4G	1	1	1	1	0	
samaung	4G	0	1	1	1	1	
Micron	4G	0	0	1	1	1	
		0	0	0	1	1	
		0	0	0	0	1	
		0	0	0	0	0	
		1	1	1	1	1	

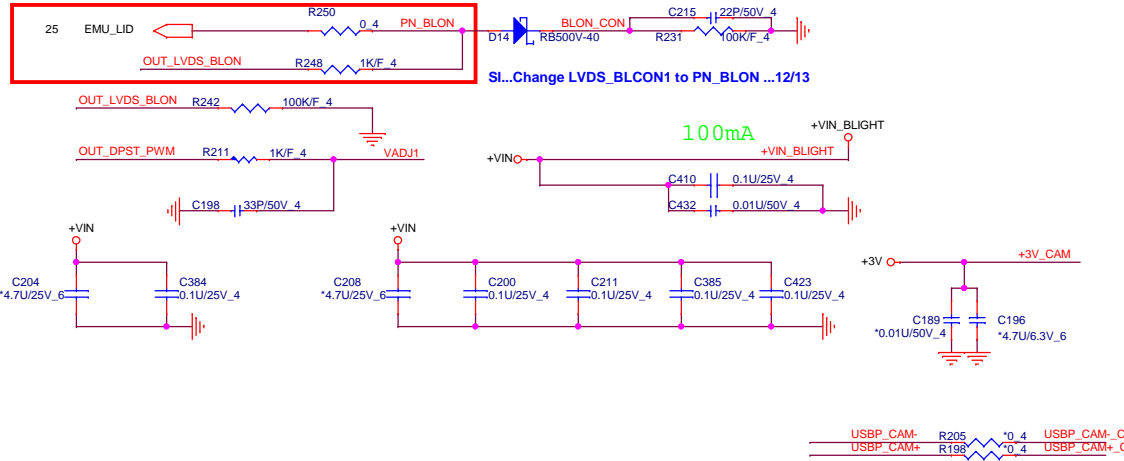




# LID Switch

LVDS Conn.

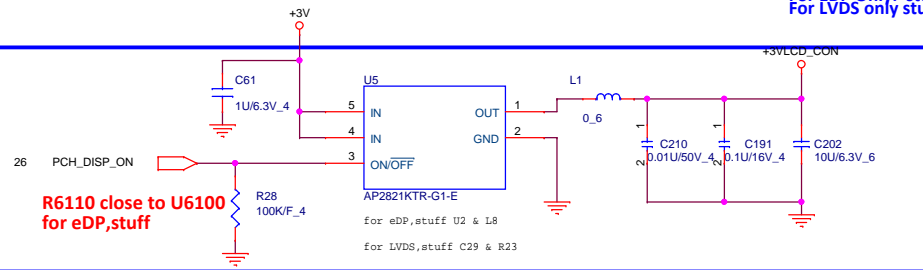
18



Sl...Change LVDS\_BLCON1 to PN\_BLON ...12/13

For EDP Only: stuff Cap  
For LVDS only stuff Resistor

For eDP

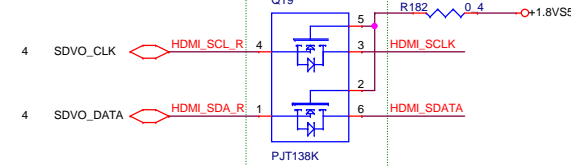


EMI Solution

HDMI SMBus Isolation

C_TX2_HDMI+	R186	150/F 2	C_TX2_HDMI-
C_TX1_HDMI+	R181	150/F 2	C_TX1_HDMI-
C_TX0_HDMI+	R189	150/F 2	C_TX0_HDMI-
C_TXC_HDMI+	R192	150/F 2	C_TXC_HDMI-

Close to HDMI connector

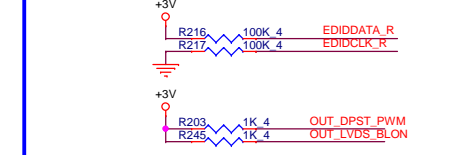


4 INT_EDP_TXP1	C206	0.1U/16V 4	TXLOUT1+
4 INT_EDP_TXN1	C203	0.1U/16V 4	TXLOUT1-
4 INT_EDP_TXN0	C193	0.1U/16V 4	TXLOUT0+
4 INT_EDP_TXP0	C192	0.1U/16V 4	TXLOUT0-
4 INT_EDP_AUXN	C194	0.1U/16V 4	EDIDDATA_R
4 INT_EDP_AUXP	C195	0.1U/16V 4	EDIDCLK_R

For EDP Only,close CN6100

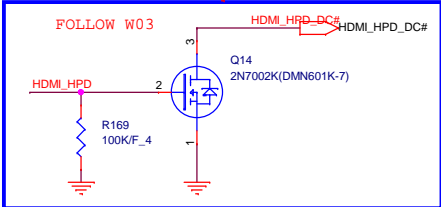
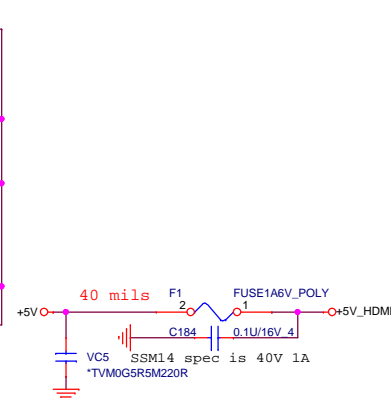
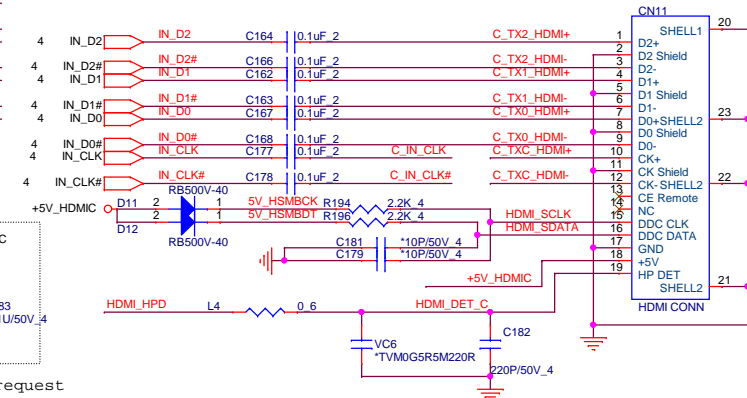
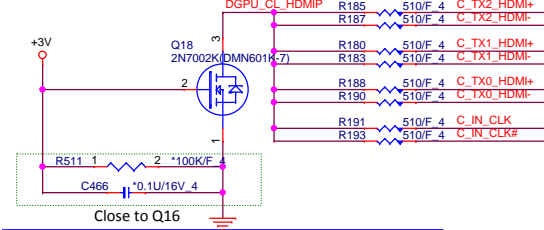


For EDP Only: Reserve

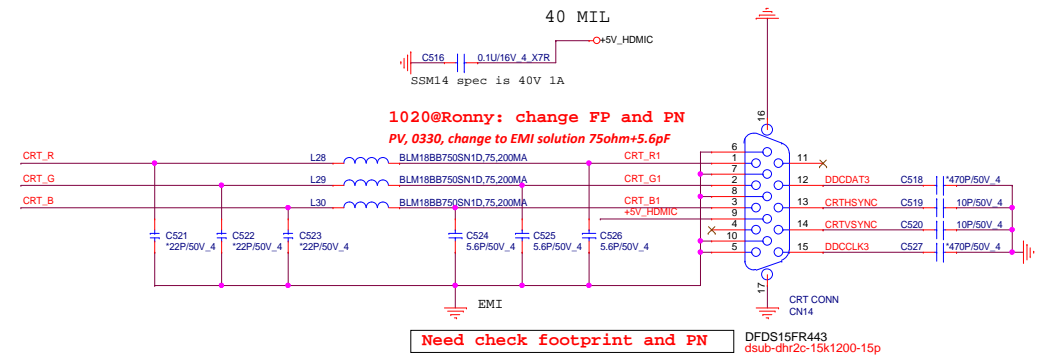
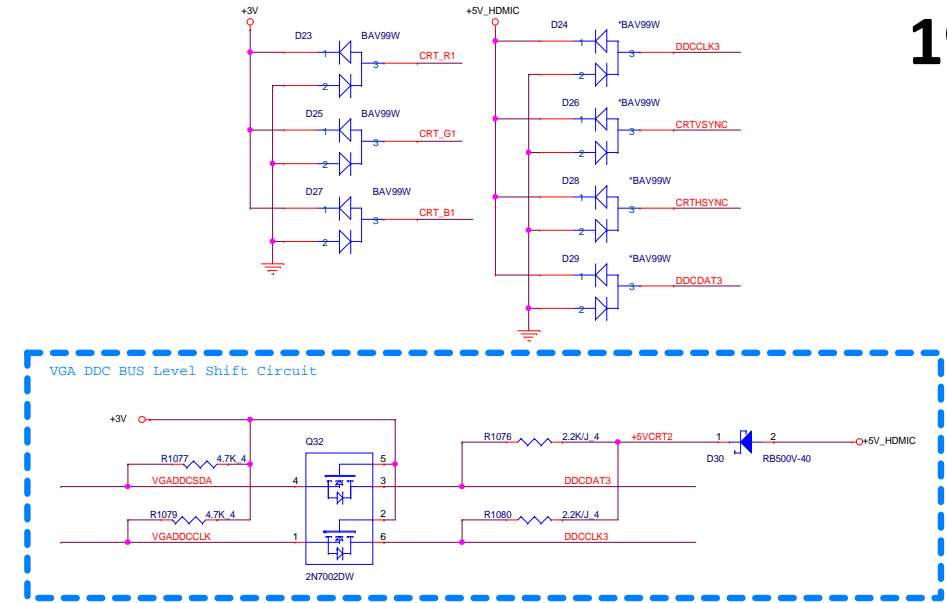
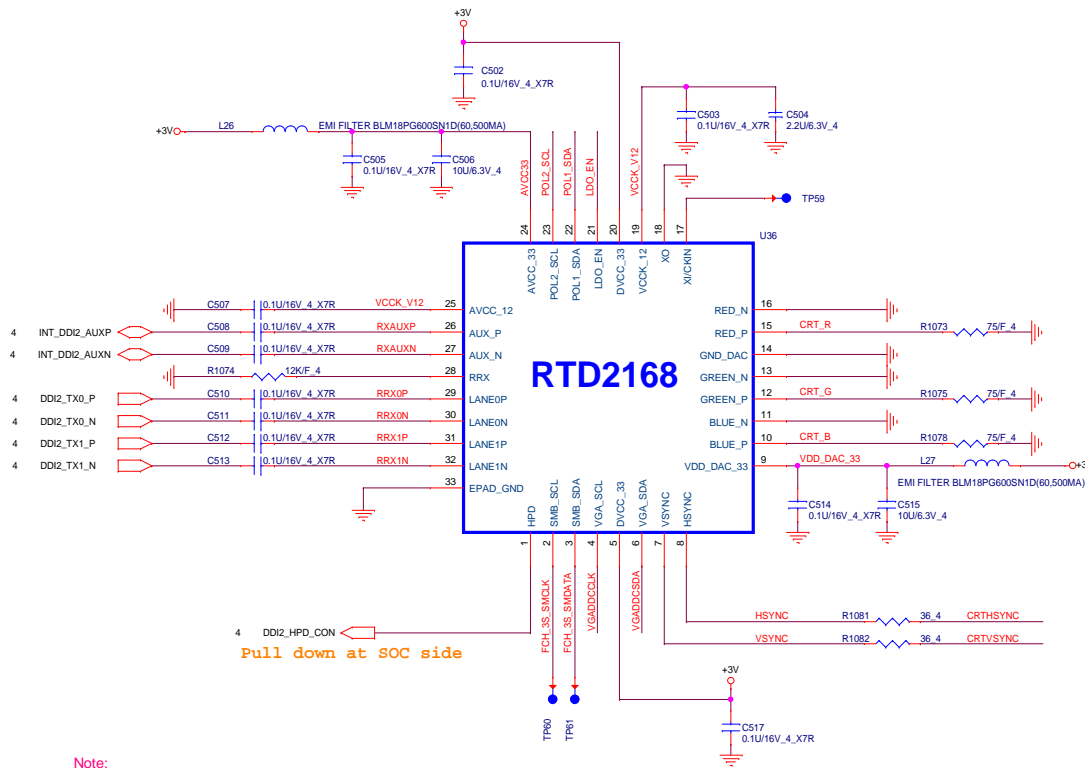


4,14,15,16,17,19,20,21,22,23,24,25,26,27,28,35	+5VS5
8,10,21,23,24,25,26,27,29,30	+3VPCU
28,29,30,31,33,34	+5V
	+VIN

Close to HDMI connector

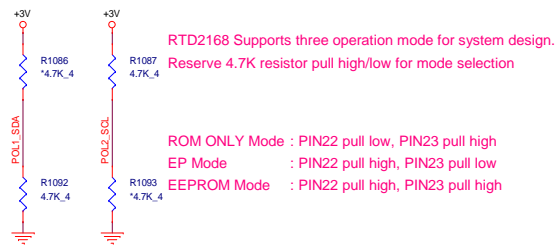


for EMI request



### Mode Configure Table(Power On Latch)

POL2_SCL(PIN23)	POL1_SDA(PIN22)	
	0	1
0	X	EP MODE
1	ROM ONLY MODE	E2PROM MODE



### EEPROM MODE

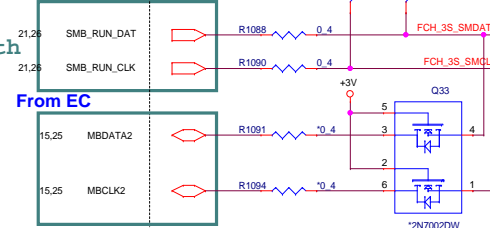
In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following conditions.

- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

DB:check with SMBUS

From PCH

From EC



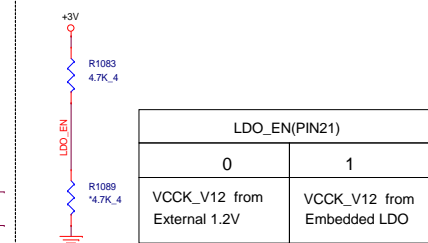
### CIIC\_SCL, CIIC\_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS  
ROM or EEPROM mode: connect to PCH SMBUS  
IIC Protocol is used

RTD2168 Slave Address:  
0x64/0x65 and 0x68/0x69

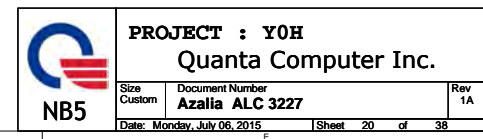
### Embedded LDO

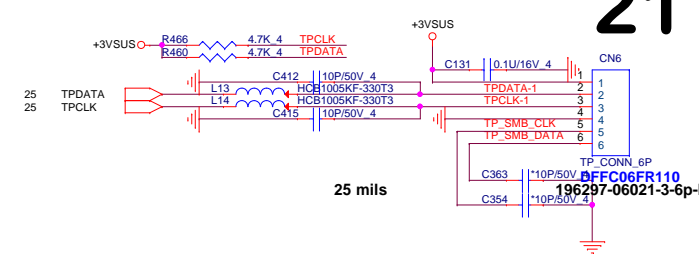
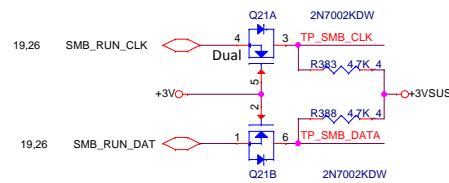
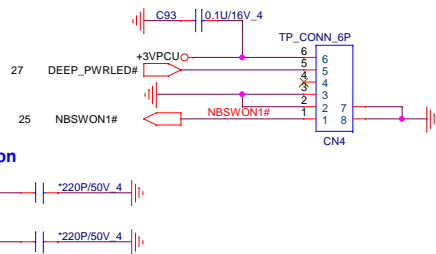
Select VCCCK\_V12 source from external 1.2V or embedded LDO



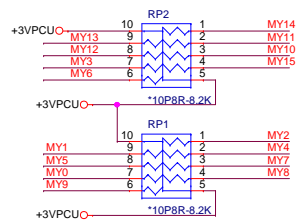
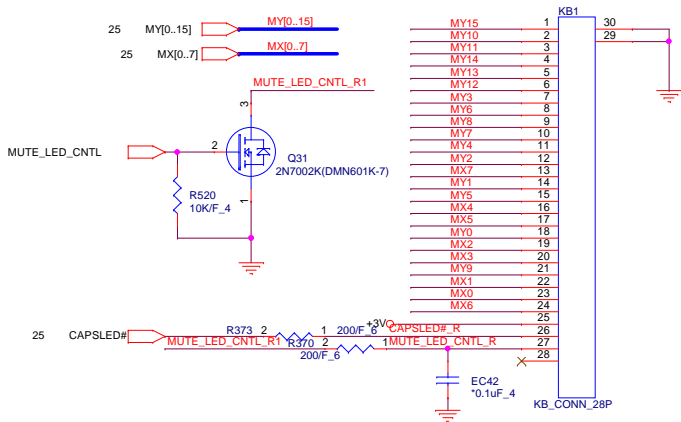
PROJECT : S400 Series  
Quanta Computer Inc.

Size Custom Document Number 27 - DP2VGA\_converter Rev 1A  
Date: Monday, July 06, 2015 Sheet 19 of 38

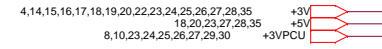
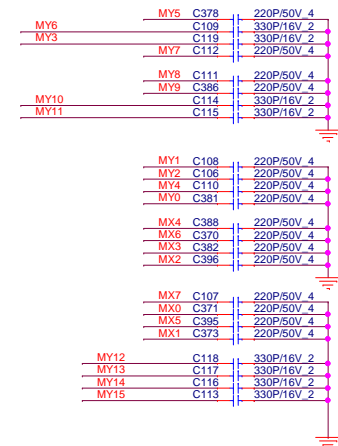




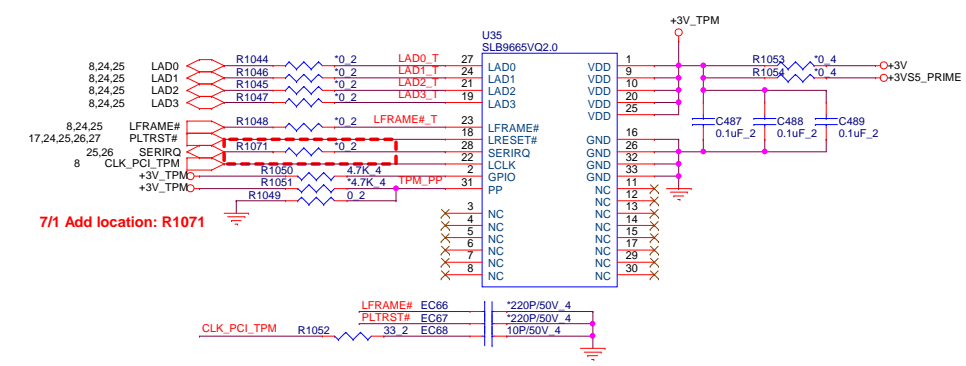
## KEYBOARD Con.



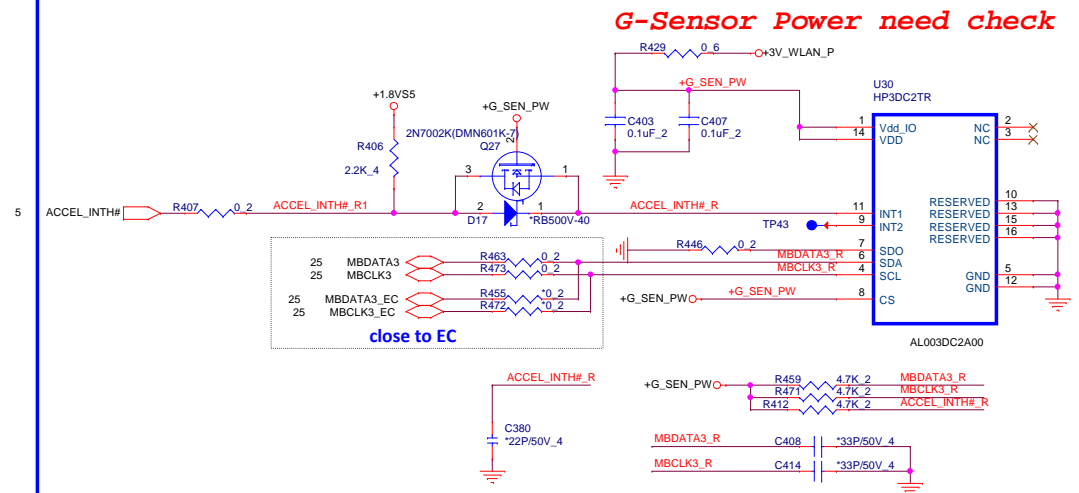
## KEYBOARD PULL-UP



TPM (2.0)



Accelerometer Sensor



Touch screen


Green CLK Circuitry

4,14,15,16,17,18,19,20,21,23,24,25,26,27,28,35  
18,20,23,27,28,35

+3V  
+5V

23,27,28,30,31,32,33,34,35  
8,10,21,23,24,25,26,27,29,30

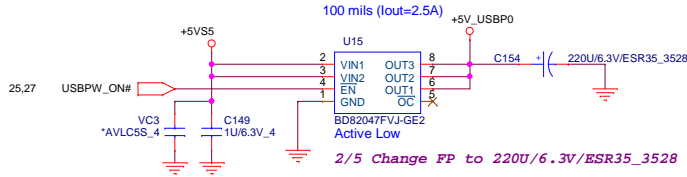
+5VS5  
+3VPCU



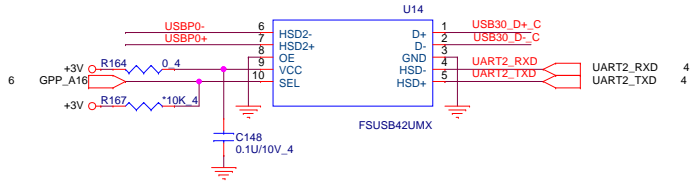
**PROJECT : Y0H**  
**Quanta Computer Inc.**

Size	Document Number USB3.0GCLK/TS/FR	Rev 1A
Date:	Monday, July 06, 2015	Sheet 22 of 38

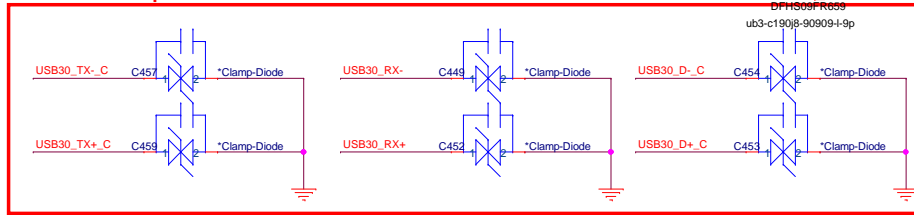
# USB 2.0/3.0 Combo



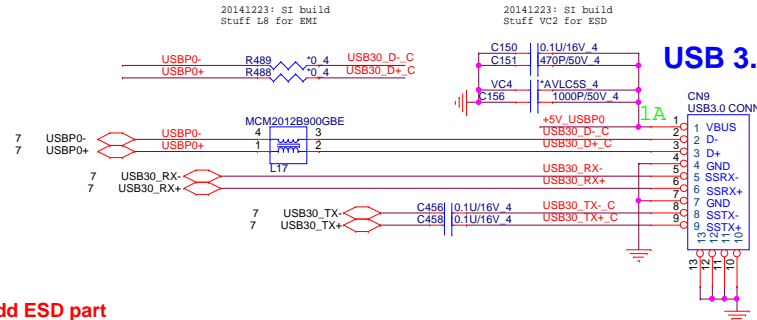
## UART for DEBUG



## 2/25 Add ESD part

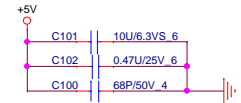
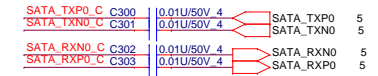
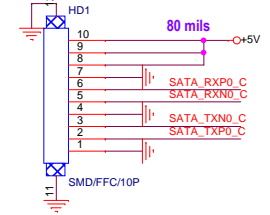


## USB 3.0

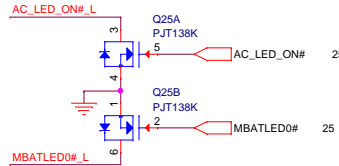


## HDD

### 3/24 Change pin define as Napa

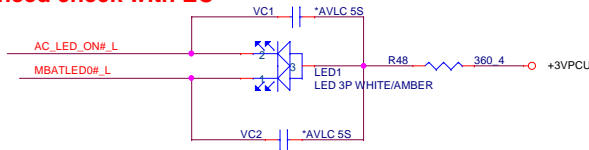


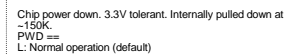
## 2/26 add LED MOS



## PWR LED

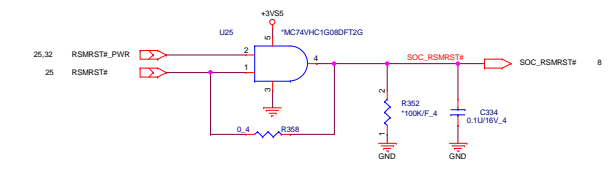
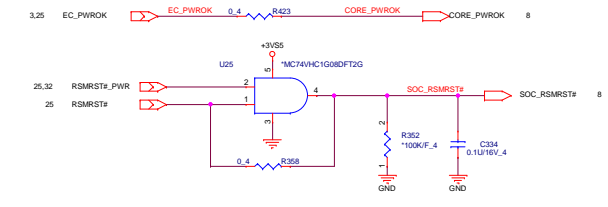
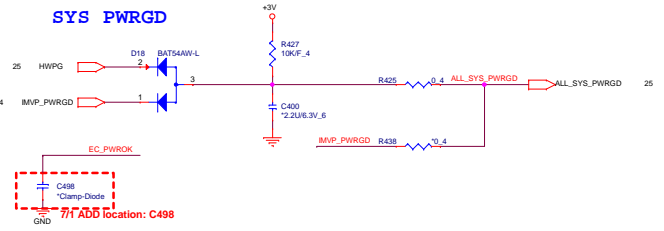
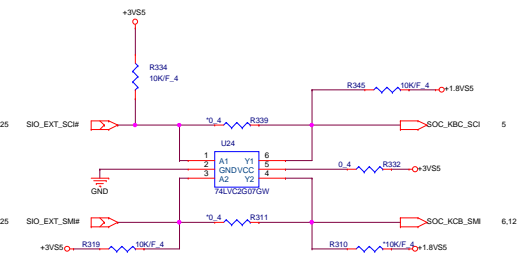
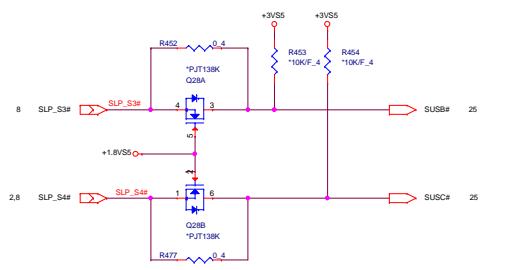
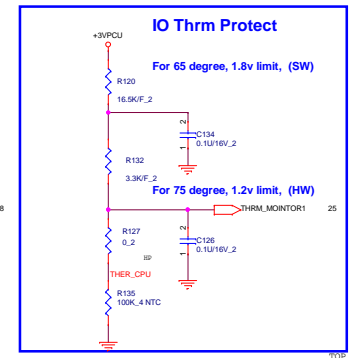
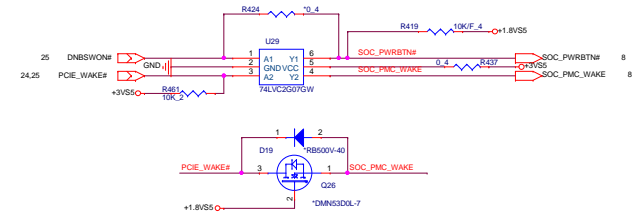
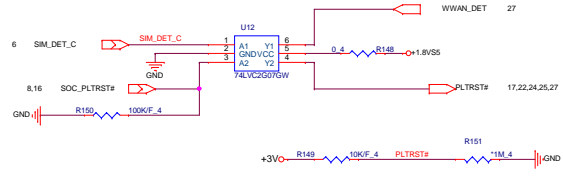
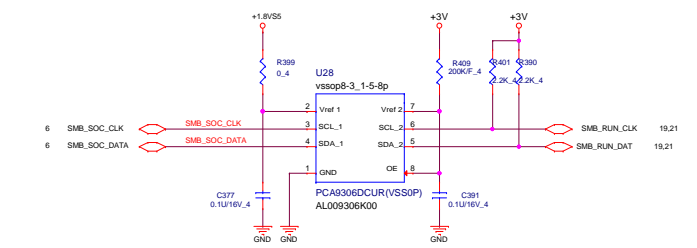
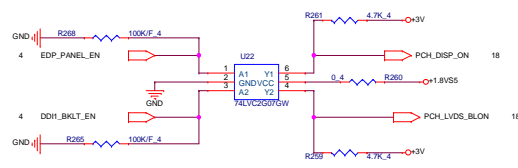
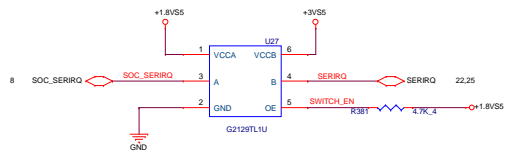
### 2/10 need check with EC



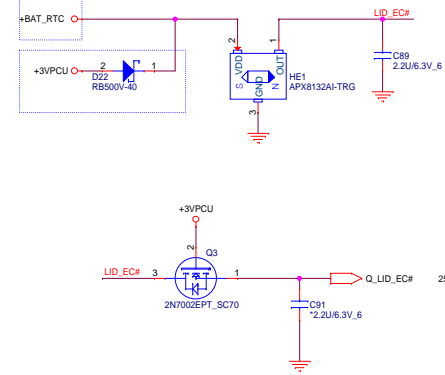




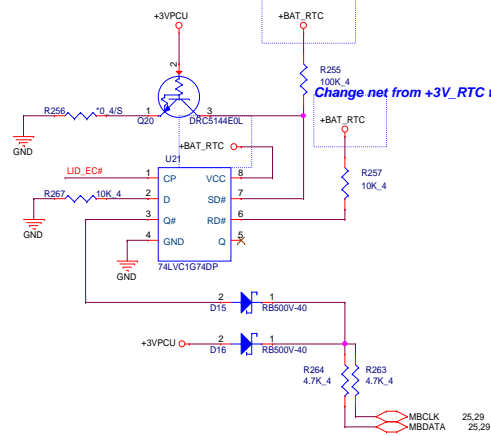




Change net from +3V\_RTC to +BAT\_RTC



Change net from +3V\_RTC to +BAT\_RTC



Input	SD	RD	CP	D	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H

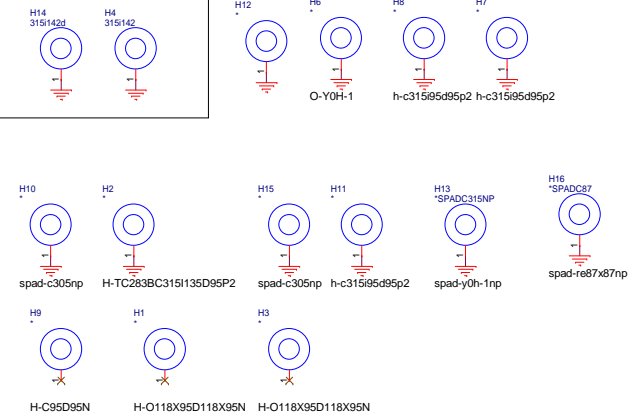
[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

Input	SD	RD	CP	D	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
H	H	↑	L	L	L	H
H	H	↑	H	H	H	L

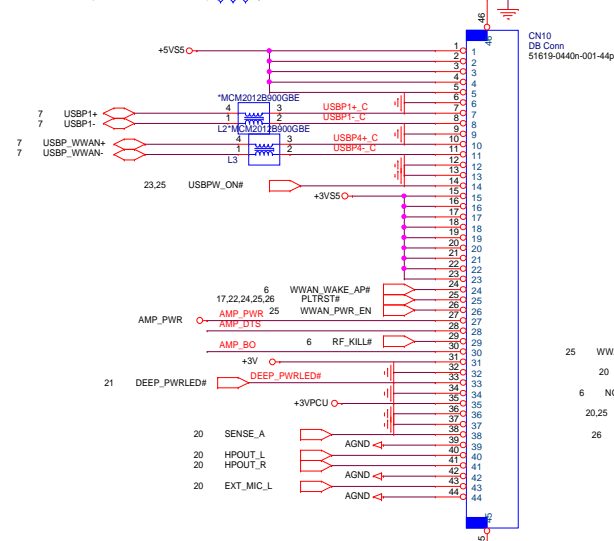
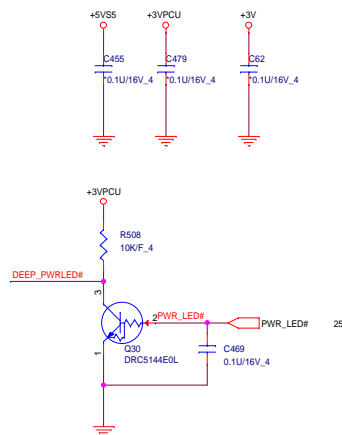
[1] H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition.

## HOLE

## Thermal Nut



## Daughter Board



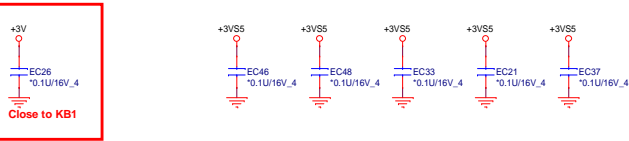
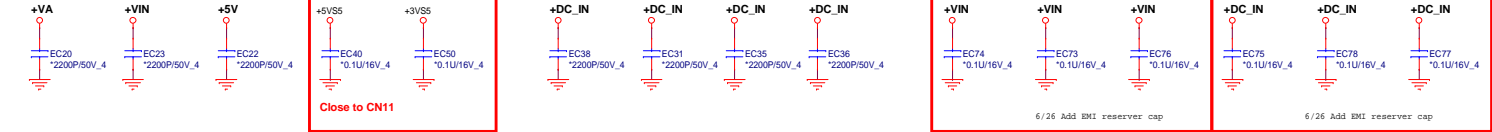
For EMI Suggestion



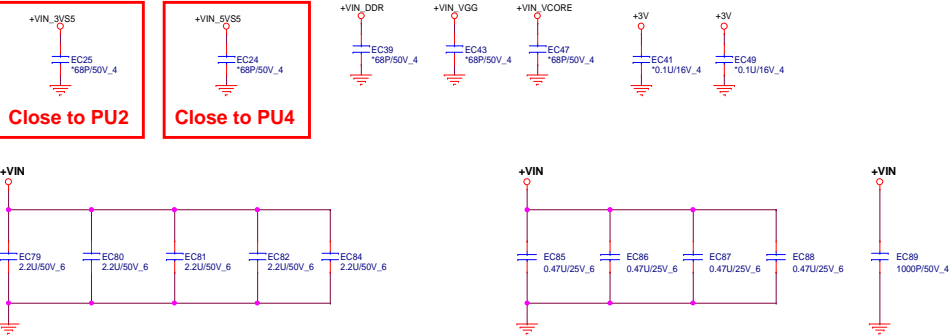
I/O port definition

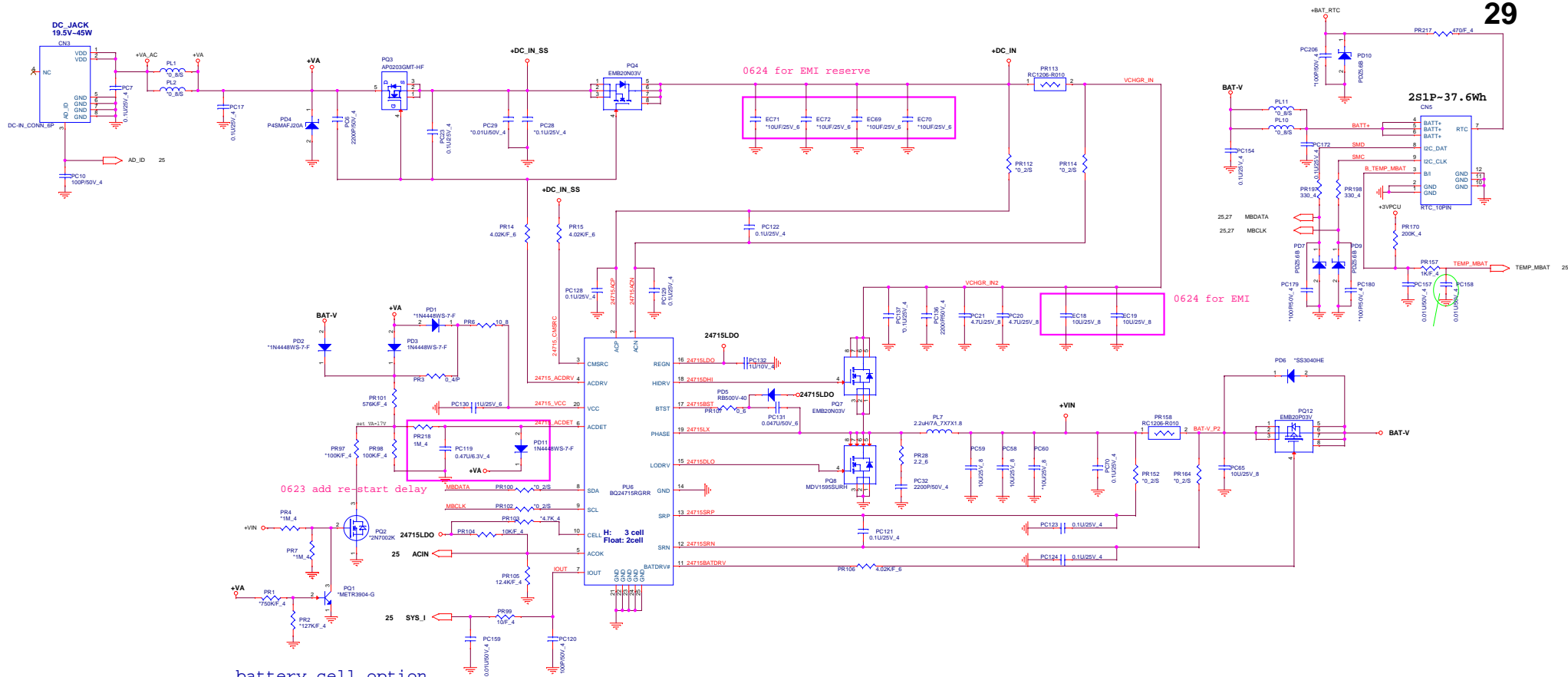
	Brasswell-M	Note
SATA Port0	HDD	
SATA Port1	ODD	
PCIE Port0	Card reader	
PCIE Port1		
PCIE Port2		
PCIE Port3	WIFI	
USB3.0 Port0	USB 2.0/3.0 Combo	
USB3.0 Port1		
USB3.0 Port2		
USB3.0 Port3		
USB2.0 Port0	USB 2.0/3.0 Combo	
USB2.0 Port1	USB 2.0	
USB2.0 Port2	Webcam	
USB2.0 Port3	BT	
USB2.0 Port4	WWAN	

EMI Reserve

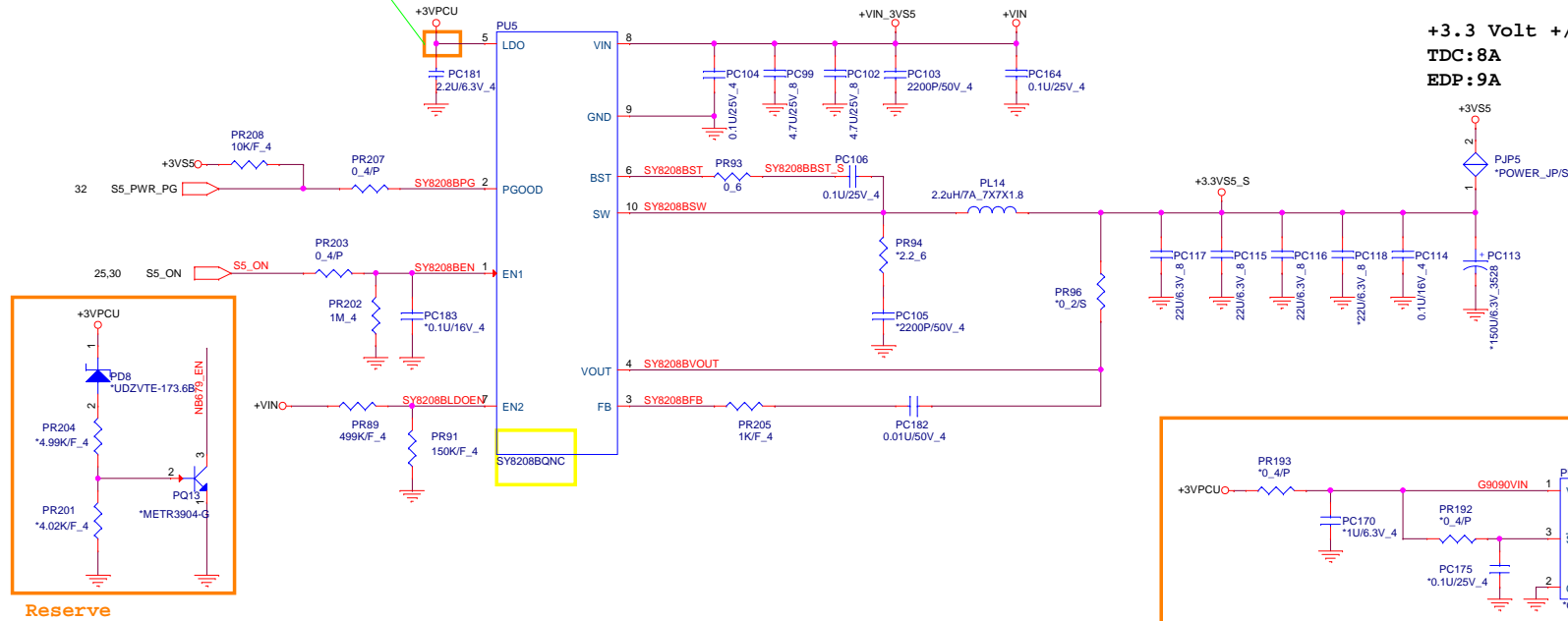


RF Reserve

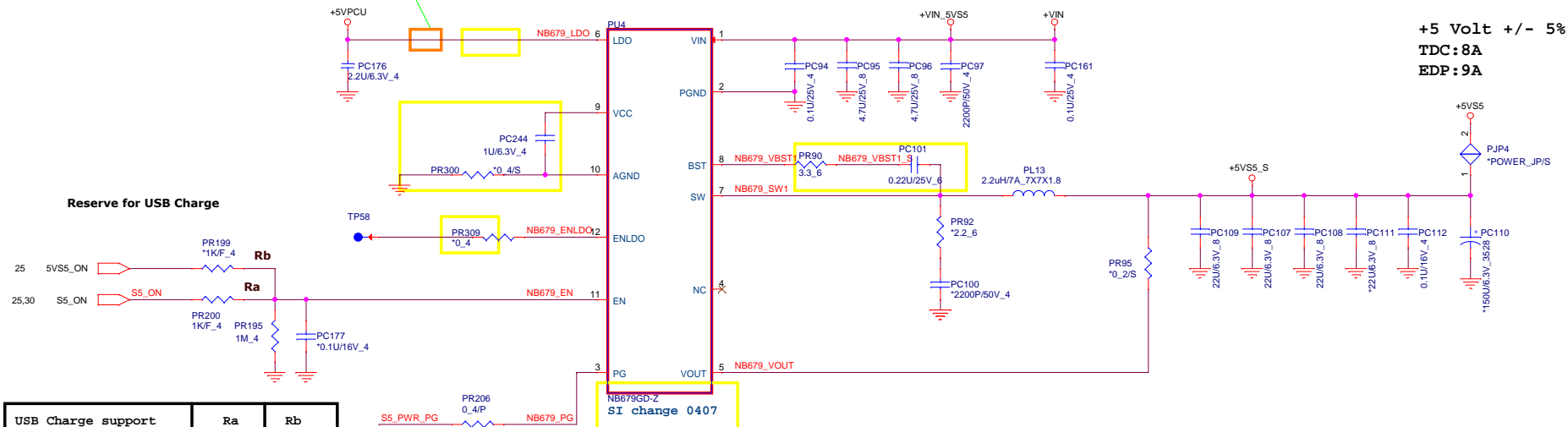




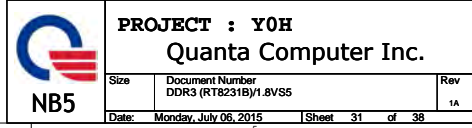
Do Not add test pad on VCC &amp; LDO pin

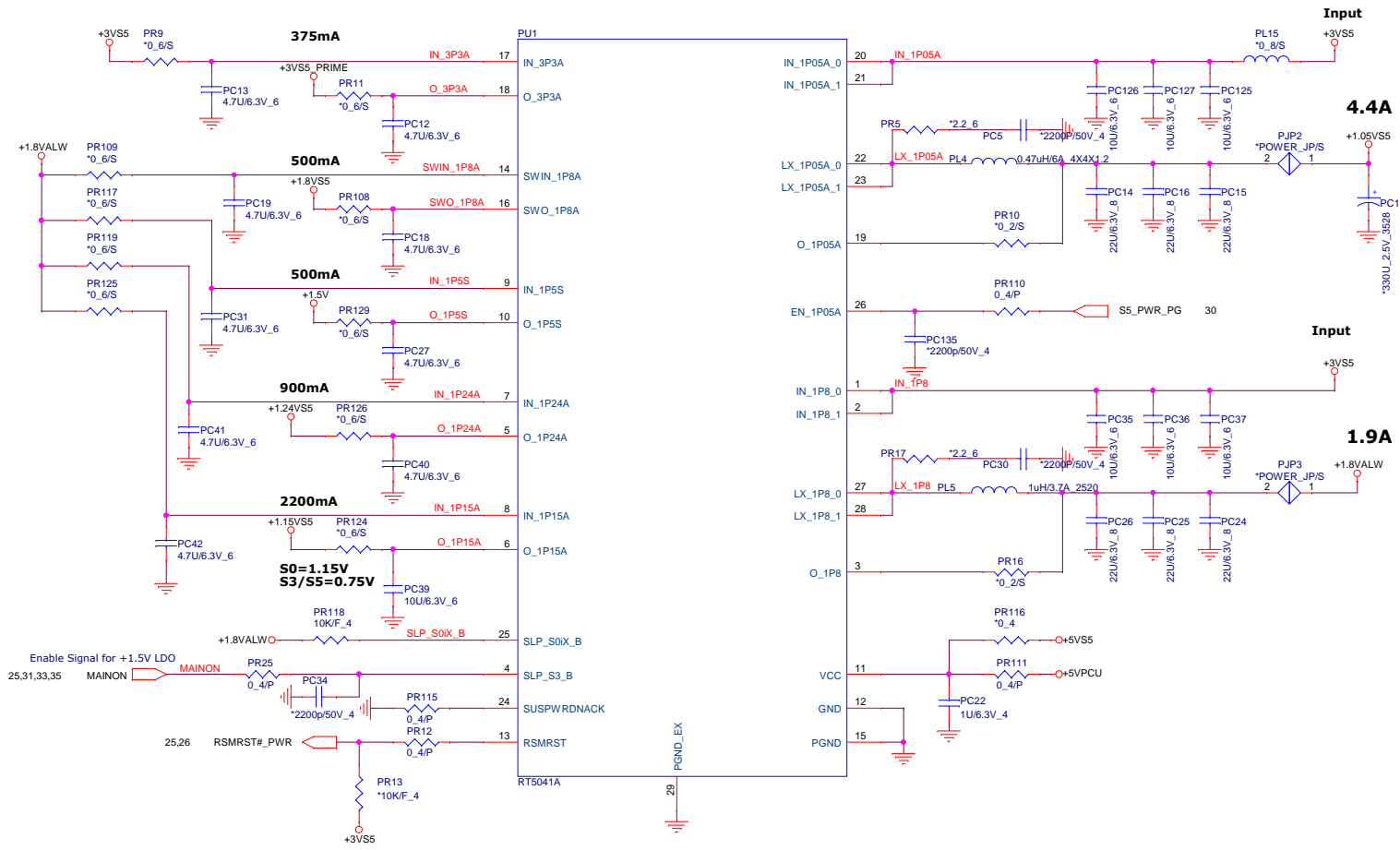


Do Not add test pad on VCC &amp; LDO pin



USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff





+3VS5	2,3,5,10,24,25,26,27,28,30,33,34,35
+1.8VALW	35
+1.8VS5	4,5,6,7,8,10,12,16,18,22,25,26,33
+3VS5_PRIME	10,22,25
+1.5V	10,20
+1.24VS5	10
+1.15VS5	9,32
+5VPCU	30,32
+1.05VS5	8,9,33,34
+1.15VS5	9,32
+5VPCU	30,32
+1.8V	4,5,35



+3VS5 2,3,5,10,24,25,26,27,28,30,32,34,35  
 +1.05VS5 8,9,32,34  
 +5VS5 23,27,28,30,31,32,34,35  
 +VGG 9  
 +1.8VS5 4,5,6,7,8,10,12,16,18,22,25,26,32  
 +VIN 18,28,29,30,31,34

